

1           1.    A method for implementing a processor-based  
2    system comprising:  
3                storing system boot instructions on a  
4    programmable, non-volatile memory coupled to a bus which is  
5    configured after the boot sequence; and  
6                accessing instructions in the memory in the  
7    process of booting the processor-based system.

1           2.    The method of claim 1 wherein storing boot  
2    instructions includes storing said instructions on a memory  
3    coupled to the peripheral component interconnect bus.

1           3.    The method of claim 1 further including storing  
2    an operating system on said non-volatile memory.

1           4.    The method of claim 1 wherein accessing  
2    instructions includes using a general purpose output pin on  
3    a chipset to supply signals to an A20GATE pin to access the  
4    memory during the process of booting the processor-based  
5    system.

1           5.    The method of claim 1 wherein storing system boot  
2    instructions includes storing the basic input/output system  
3    on said memory.

1           6.    The method of claim 1 further including modifying  
2    the address of the boot device.

1           7.    The method of claim 6 further including causing a  
2    legacy bus controller to ignore said address.

1           8.    The method of claim 8 further including causing a  
2    controller associated with said memory to respond to said  
3    address.

1           9.    A processor-based system comprising:  
2                a processor;  
3                a volatile memory coupled to said processor;  
4                a peripheral component interconnect bus coupled  
5    to said processor; and  
6                a non-volatile memory coupled to said bus storing  
7    system boot instructions.

1           10.   The system of claim 9 wherein said system boot  
2    instructions include the basic input/output system for said  
3    processor-based system.

1           11.   The system of claim 10 wherein said non-volatile  
2    memory is a FLASH memory.

1           12.   The system of claim 9 including a chipset coupled  
2    to said bus and having a general purpose output pin and an  
3    A20GATE pin, the general purpose output pin coupled to said  
4    A20GATE pin.

1           13. The system of claim 12 wherein said A20GATE pin  
2           is adapted to create a unique boot address for said non-  
3           volatile memory.

1           14. A memory adapted to be coupled to a peripheral  
2           component interconnect bus comprising:  
3                   a non-volatile, re-programmable semiconductor  
4           memory array storing a basic input/output system; and  
5                   a peripheral component interconnect bus  
6           controller coupled to said memory array.

1           15. The memory of claim 14 wherein said memory is a  
2           FLASH memory.

1           16. The memory of claim 13 wherein said controller is  
2           configured to respond as the boot device.

1           17. The memory of claim 13 wherein said controller is  
2           not configured to respond as the boot device.

1           18. The memory of claim 13 wherein said array stores  
2           an operating system.

1           19. The memory of claim 13 wherein said memory is  
2           adapted to be re-programmed without user intervention.

1           20. The memory of claim 13 including a controller  
2   adapted to respond as the boot device.